

REVISION HISTORY

| REV | DESCRIPTION | ZONE |
|-----|-------------|------|
|     |             |      |

FABRICATION NOTES (UNLESS OTHERWISE SPECIFIED)

- 1) FABRICATE PER IPC-6012A CLASS 2.
- 2) OUTLINE DEFINED IN SEPARATE GERBER FILE WITH "Edge\_Cuts.GBR" SUFFIX.
- 3) SEE SEPARATE DRILL FILES WITH ".DRL" SUFFIX FOR HOLE LOCATIONS.

SELECTED HOLE LOCATIONS SHOWN ON THIS DRAWING FOR REFERENCE ONLY.

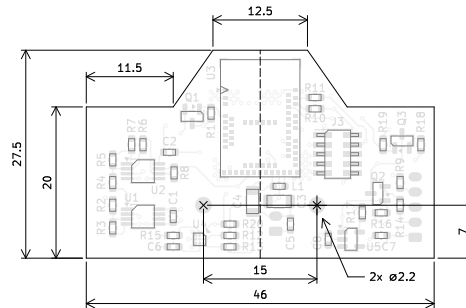
- 4) SURFACE FINISH: HAL SNPB
- 5) SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR GREEN.
- 6) SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.
- 7) ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
- 8) RESERVED
- 9) PCB MATERIAL REQUIREMENTS:
  - A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS.
  - B. Tg 135 C OR EQUIVALENT.

10) DESIGN GEOMETRY MINIMUM FEATURE SIZES:

|                  |                    |
|------------------|--------------------|
| BOARD SIZE       | 46.000 × 27.500 mm |
| BOARD THICKNESS  | 1.647 mm           |
| TRACE WIDTH      | 0.100 mm           |
| TRACE TO TRACE   | 0.200 mm           |
| MIN. HOLE (PTH)  | 0.300 mm           |
| MIN. HOLE (NPTH) | 2.200 mm           |
| ANNULAR RING     | 0.150 mm           |
| COPPER TO HOLE   | 0.250 mm           |
| COPPER TO EDGE   | 0.500 mm           |
| HOLE TO HOLE     | 0.250 mm           |

- 11) ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
- 12) FOR REFERENCE ONLY THE STACKUP CORRESPONDS TO JLCPCB STACKUP JLC04161H-7628.  
FOR REFERENCE ONLY. IMPEDANCE IS THE CONTROLLING PARAMETER OVER LAYER STACKUP. GERBER DATA MAY NOT BE ALTERED EXCEPT FOR STANDARD FABRICATION ALLOWANCES.

THE SUPPLIED ARTWORK MAY OR MAY NOT CONTAIN THE SPECIFIED TRACE GEOMETRIES ON EVERY LAYERS SPECIFIED.



All dimensions are in millimeters unless otherwise specified.

Stackup Table

| Material | Layer        | Thickness         | Dielectric | Type        |
|----------|--------------|-------------------|------------|-------------|
|          | F.Paste      |                   |            | Paste Mask  |
|          | F.Silkscreen |                   |            | Legend      |
|          | F.Mask       | 0.0305mm          |            | Solder Mask |
| Copper   | F.Cu         | 0.035mm (1.00oz)  |            | Signal      |
| Prepreg  |              | 0.2104mm          | FR4        | Dielectric  |
| Copper   | In1.Cu       | 0.0152mm (0.43oz) |            | Signal      |
| Core     |              | 1.065mm           | FR4        | Dielectric  |
| Copper   | In2.Cu       | 0.0152mm (0.43oz) |            | Plane       |
| Prepreg  |              | 0.2104mm          | FR4        | Dielectric  |
| Copper   | B.Cu         | 0.035mm (1.00oz)  |            | Plane       |
|          | B.Mask       | 0.0305mm          |            | Solder Mask |
|          | B.Silkscreen |                   |            | Legend      |
|          | B.Paste      |                   |            | Paste Mask  |

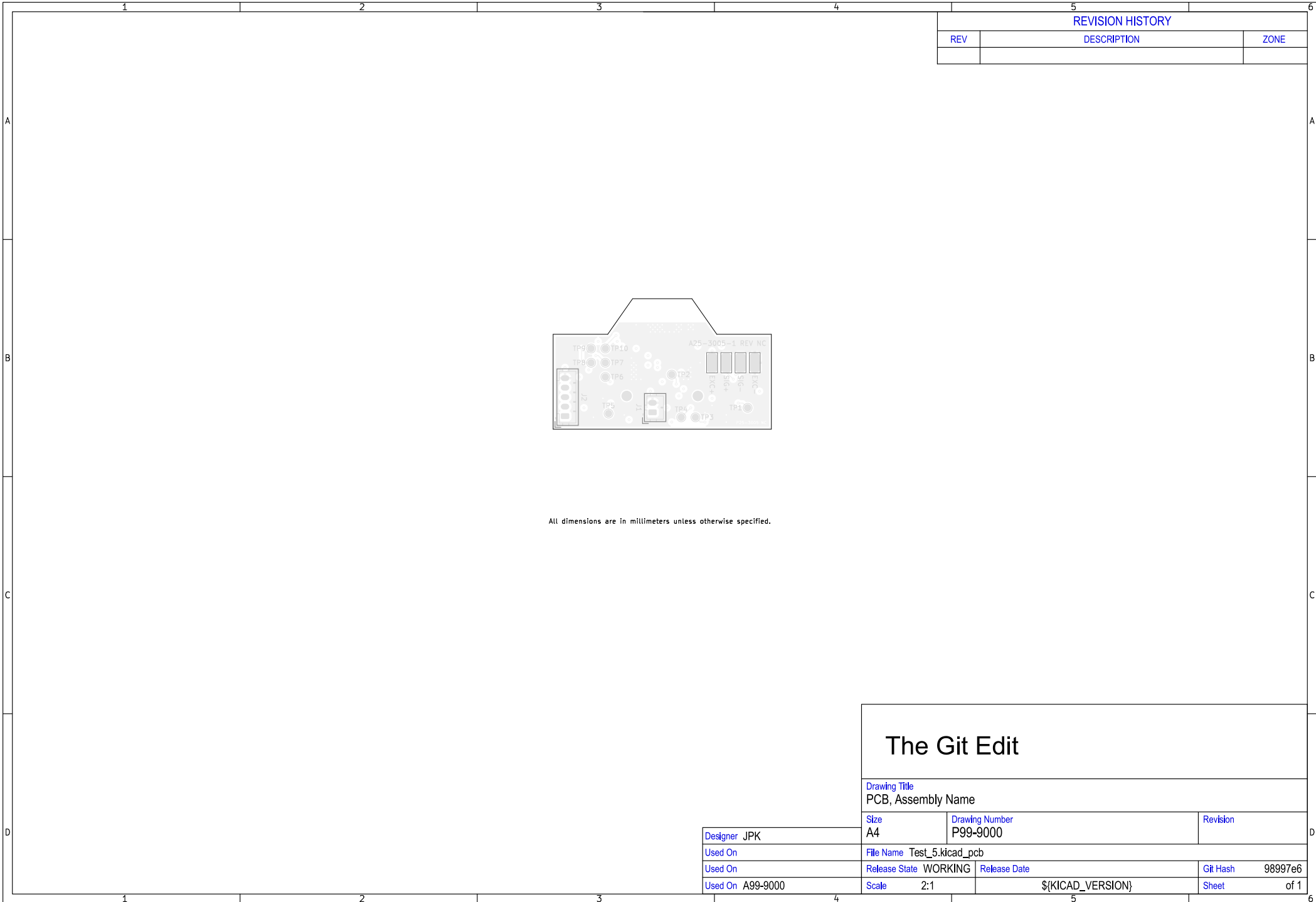
Total thickness: 1.6472mm  
Note: external layer thicknesses are specified after plating

Impedance Table

| Layer | Ref1 | Ref2 | Type | Impedance | Width | Space | Tolerance |
|-------|------|------|------|-----------|-------|-------|-----------|
| L1    | AIR  | L2   | SE   | 50        | 0.350 | —     | 10%       |
| L1    | AIR  | L2   | DIFF | 90        | 0.286 | 0.203 | 10%       |
| L1    | AIR  | L2   | DIFF | 100       | 0.220 | 0.203 | 10%       |

The Git Edit

|                                     |                               |                 |                     |
|-------------------------------------|-------------------------------|-----------------|---------------------|
| Drawing Title<br>PCB, Assembly Name |                               |                 |                     |
| Size<br>A4                          | Drawing Number<br>P99-9000    |                 | Revision            |
| Designer<br>JPK                     | File Name<br>Test_5.kicad_pcb |                 |                     |
| Used On                             | Release State<br>WORKING      | Release Date    | Git Hash<br>98997e6 |
| Used On<br>A99-9000                 | Scale<br>2:1                  | {KICAD_VERSION} | Sheet<br>of 1       |



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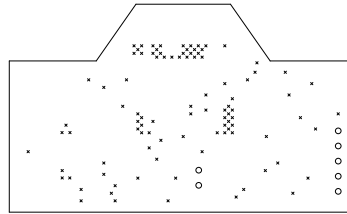
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|                                     |                               |                                   |                     |
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**Drill Table**

| Symbol | Count     | Hole Size          | Plated | Hole Shape | Drill Layer Pair | Hole Type |
|--------|-----------|--------------------|--------|------------|------------------|-----------|
| ×      | 97        | 0.30mm (11.81mils) | PTH    | Round      | F,Cu - B,Cu      | Via       |
| ○      | 7         | 0.75mm (29.53mils) | PTH    | Round      | F,Cu - B,Cu      | Pad       |
|        | Total 104 |                    |        |            |                  |           |



# The Git Edit

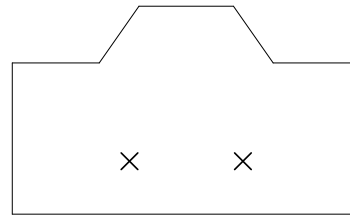
|                                     |                            |              |                  |
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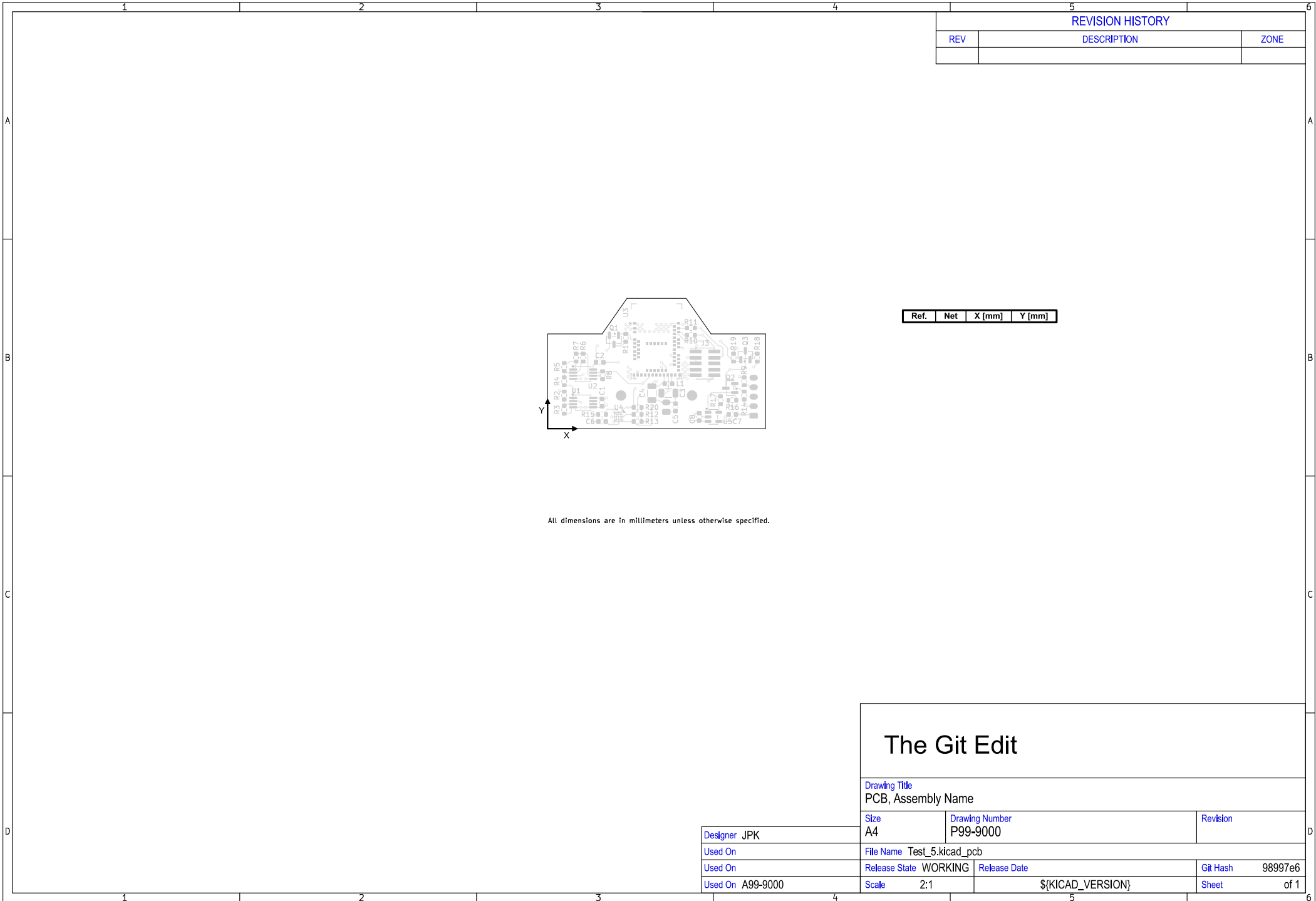
Drill Table

| Symbol | Count   | Hole Size          | Plated | Hole Shape | Drill Layer Pair | Hole Type  |
|--------|---------|--------------------|--------|------------|------------------|------------|
| ×      | 2       | 2.20mm (86,61mils) | NPTH   | Round      | F,Cu - B,Cu      | Mechanical |
|        | Total 2 |                    |        |            |                  |            |



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|                                     |                            |              |                  |
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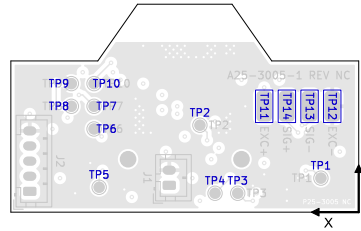


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| Ref. | Net            | X [mm] | Y [mm] |
|------|----------------|--------|--------|
| TP1  | Net-(U1A-)     | 5.00   | 4.50   |
| TP2  | LOAD_CELL      | 21.00  | 11.50  |
| TP3  | Net-(J1-Pin_1) | 16.00  | 2.50   |
| TP4  | BATT_INT       | 19.00  | 2.50   |
| TP5  | STAT           | 34.32  | 3.29   |
| TP6  | RESET          | 35.00  | 11.00  |
| TP7  | SWDCLK         | 35.00  | 14.00  |
| TP8  | +3.3V          | 38.00  | 14.00  |
| TP9  | GND            | 38.00  | 17.00  |
| TP10 | SWDIO          | 35.00  | 17.00  |
| TP11 | EXC+           | 12.50  | 14.00  |
| TP12 | GND            | 3.50   | 14.00  |
| TP13 | SIG+           | 6.50   | 14.00  |
| TP14 | SIG-           | 9.50   | 14.00  |

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## The Git Edit

Drawing Title

PCB, Assembly Name

Size

A4

Drawing Number

P99-9000

Revision

Designer JPK

Used On

File Name Test\_5.kicad\_pcb

Used On

Release State WORKING

Release Date

Git Hash 98997e6

Used On A99-9000

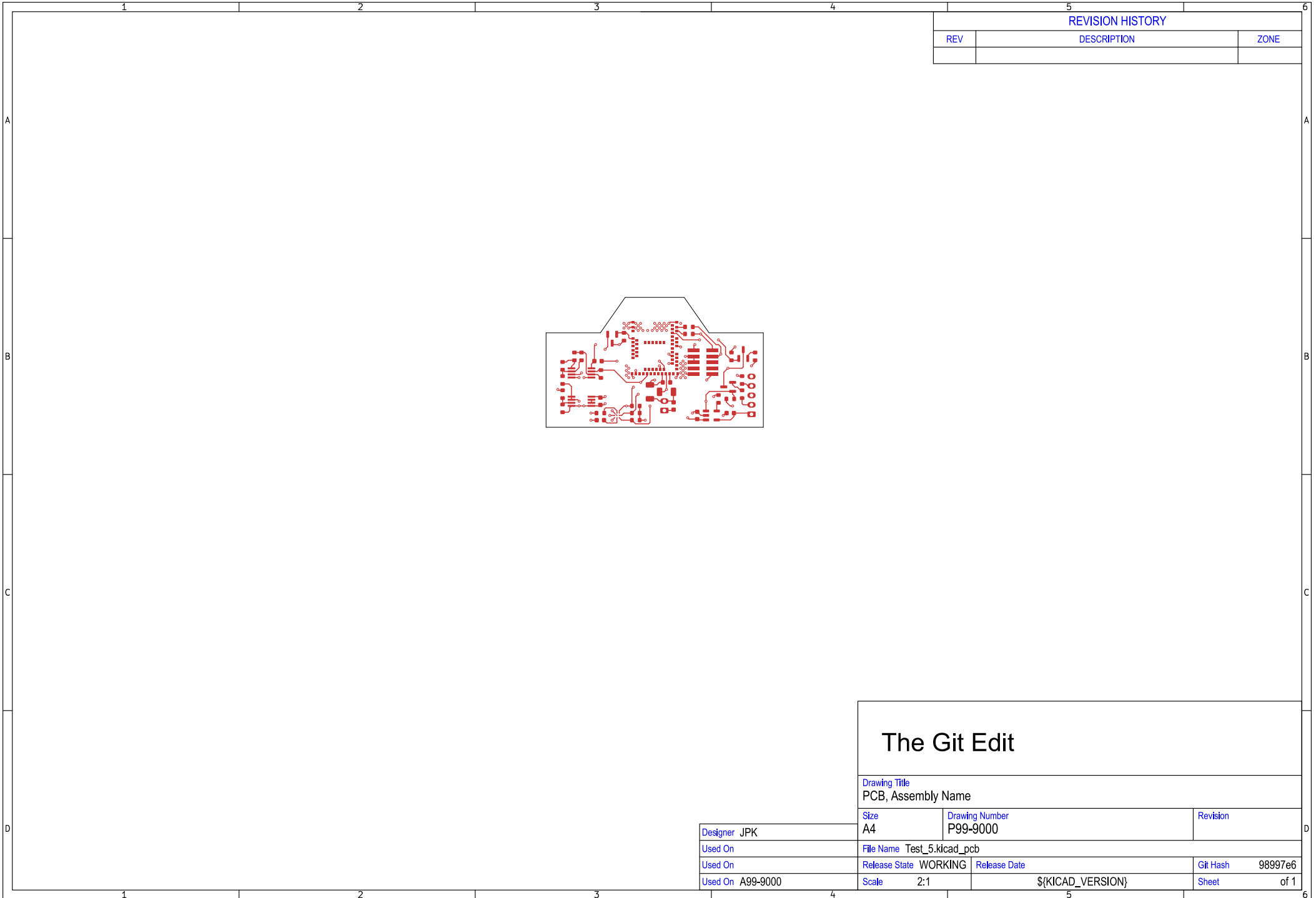
Scale

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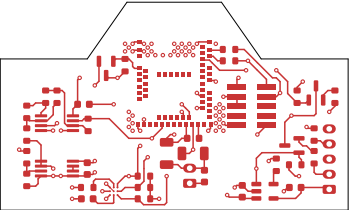
\${KICAD\_VERSION}

Sheet

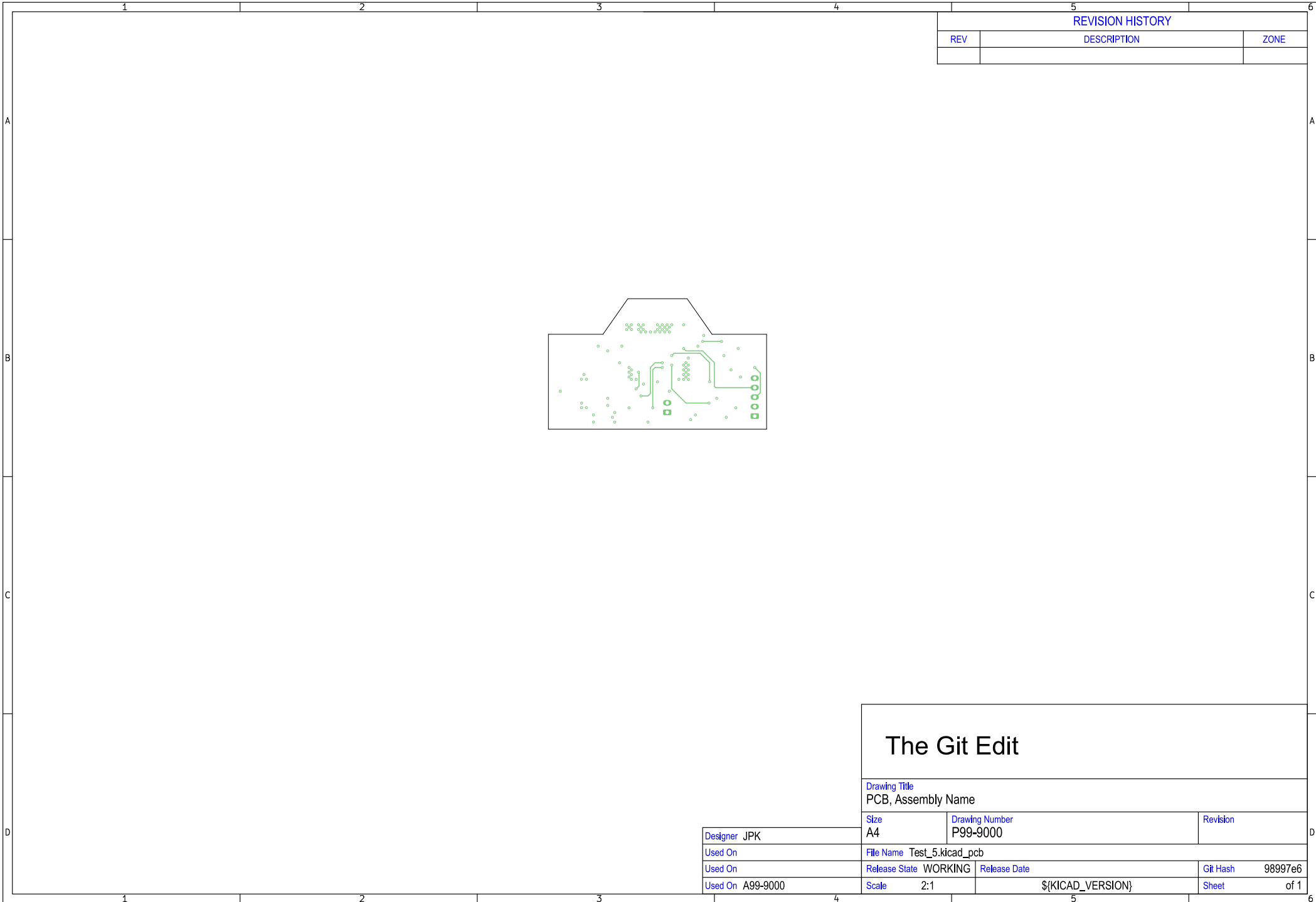
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| <h1>The Git Edit</h1>               |                               |                          |              |
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